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Anomalous Behavior of Synchronizer and Arbiter Circuits

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Abstract—Observations are shown of oscillatory and metastable behavior of flip-flops in response to logically undefined input conditions such as those that occur in synchronizers and arbiters. Significant systems failures have resulted from this fundamentally inescapable problem that is generally not appreciated by system designers and users.

Index Terms—Asynchronous interactions, binary switching time, flip-flop metastable region, interrupt failure, synchronizer failure mode.

Discussion at a recent Workshop on Synchronizer Failures (Washington University, St. Louis, Mo.; April 27–28, 1972) has revealed that a number of computer systems made by several manufacturers are subject to significant rates of system failure that result from unreliable interactions between mutually asynchronous subsystems. Multiprocessor systems currently under development may be particularly vulnerable to synchronizer failure mechanisms that are apparently not generally appreciated by system designers and users. When arranging for intercommunication between two subsystems that do not share a common time reference, it is impossible to avoid the generation of signals (sometimes called split pulses or runt pulses) that are not logically defined. The conventional solution [1] is to use these signals as inputs to a synchronizing element, typically a flip-flop, and to assume that the flip-flop output reaches a logically defined state within some maximum fixed time after the input occurs.

The authors [4], [5] and others [2], [3] have been aware for some time that this assumption is false, and that there is no fixed time interval sufficiently long to ensure that the flip-flop will, with probability one, reach a defined output state. However, the recent evidence of system failures prompts us to call attention to some observations that have been made of the modes of anomalous output behavior of certain commonly used flip-flops in response to inputs similar to those that would occur when using these circuits as synchronizer elements [6]. The observations shown required care in circuit design and layout in order to achieve the repeatability needed to photograph the events.

In one such mode of flip-flop behavior, illustrated by Figs. 1 and 2, the output hovers for an indeterminate time at a metastable value somewhere intermediate between the defined 0 and 1 output levels. This mode is typical of flip-flop circuits that have a small signal-propagation time to signal-rise time ratio. The figures show the response of an emitter-coupled logic (ECL) clocked *R-S* flip-flop (Motorola MC1016) when the clock input signal is switched off as the data input signal is changing. Fig. 1 is a 5-min exposure of a sampling oscilloscope display of Q and \bar{Q} ; while Fig. 2, from a real time oscilloscope, shows the details of some individual output trajectories.

In another anomalous mode of behavior, shown in Figs. 3 and 4, the Q and \bar{Q} outputs oscillate in phase a number of times between the 0 and 1 state before finally coming to rest out of phase. This mode is typical of flip-flops constructed from gates with larger propagation time to rise time ratios. Transistor-transistor logic (TTL) *R-S*-type flip-flops are often constructed by cross tying two NAND gates. Fig. 3 shows the resulting behavior when the *R* and *S* inputs of an *R-S* flip-flop constructed from two gates in a SN7410 package are switched high at the same time. Fig. 4, a real-time display of another TTL *R-S*

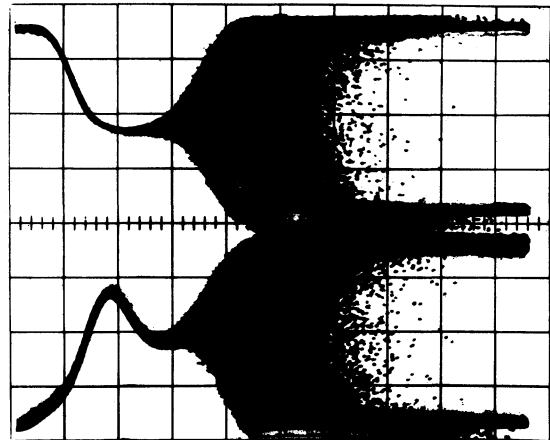


Fig. 1. Q and \bar{Q} of ECL clocked *R-S* flip-flop with clock and data inputs changing simultaneously (5 ns/div, 0.25 V/div).

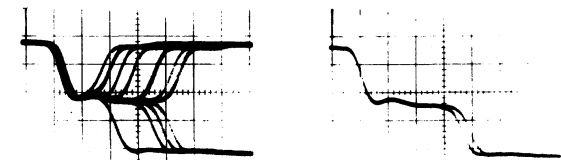


Fig. 2. Selected responses of ECL clocked *R-S* flip-flop to clock and data inputs changing simultaneously (10 ns/div, 0.2V/div).

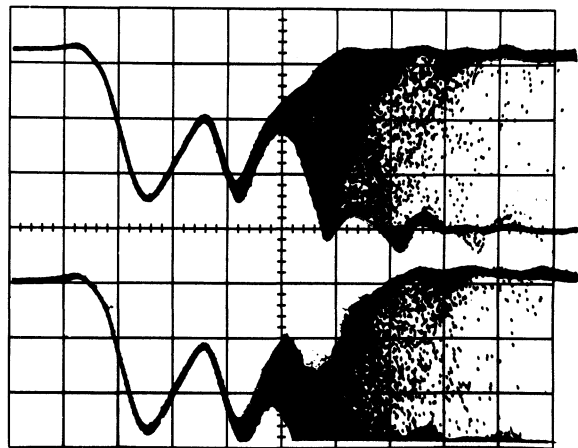


Fig. 3. Q and \bar{Q} TTL cross-tied NAND gates (SN7410) with the *R* and *S* inputs switched high simultaneously (5 ns/div, 1V/div).

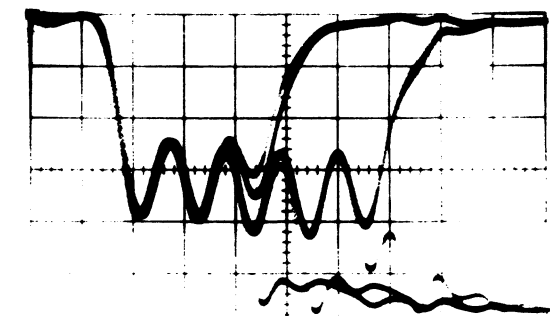


Fig. 4. Selected responses of TTL cross-tied NAND gates (SN7400) with a runt pulse applied to the *R* input (10 ns/div, 1V/div).

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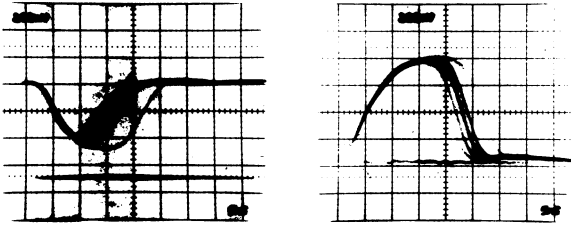


Fig. 5. Selected responses of SN7474 TTL flip-flop with the clock and data input signals carefully adjusted. Left Q , right \bar{Q} (5 ns/div, 1V/div).

flip-flop, shows the behavior when a runt pulse is supplied to the R input. Note that the oscillation continues until the flip-flop settles.

Because it has been widely used as a synchronizer element, we observed the behavior of a SN7474-type D -edge triggered latch made up of three internally interconnected R - S flip-flops. Three different relationships of time and phase between the clock and data input signals produced anomalous behavior. Two relationships: 1) the clock and data signals both switching high at almost the same time; and 2) the data signal switching high approximately 3 ns before the clock signal switched high, produced longer than normal propagation times that varied from trial to trial. When the outputs did begin to switch, they always switched fully from one state to the other with a normal rise time. The third input condition, with the data switching low approximately 3 ns before the clock signal switched high, produced pulses of variable width at the outputs as shown in Fig. 5.

We feel that it is important that computer system and circuit designers recognize the fundamental nature of this problem, and that computer programmers and users should be aware of this relatively obscure, and difficult to pinpoint failure mechanism that may account for some fraction of previously unexplainable system crashes. It is surprising that there is little literature on this topic and we are unaware of any commercially available integrated circuit flip-flop that is specified in a manner that makes it possible to predict its failure probability as a synchronizing element. We have found only scattered instances in which the possibility of this type of failure has been taken into account by designers in estimating the reliability of their systems.

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An Equational Axiomatization for the Disjoint System of Post Algebras

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Abstract—It is shown that the class of Post algebras of finite order n is equationally definable where the only unary operators are the disjoint operators C_i , $i = 0, 1, \dots, n-1$.

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Index Terms—Disjoint system of Post algebras, generalized monotonic system of Post algebras, generalized Post algebras, monotonic system of Post algebras, multiple-valued logic design, Post algebras, ternary switching theory.

I. INTRODUCTION

There has been recent interest in both the disjoint and monotonic systems of Post algebras. An axiomatization for the former system appears in [1]; an axiomatization for the latter system appears in [2]. Since a feature of equational axiomatization is that it throws maximum emphasis on essential properties of the unary operators that are employed, the following correspondence provides such an axiomatization for the disjoint system of Post algebras.

Thus basic properties of the disjoint unary operators are given from which all other properties of these operators may be obtained. This result is of interest with respect to recent work in generalized Post algebras, which ensures only monotonic representations and hence is a generalization of the monotonic system of Post algebras [3]. Generalization of Post algebras that ensures disjoint representations is important for considerations of logical design, and plays a role in [6], for example.

A bibliography for mathematical references may be found in [5]. Applications may be found in various papers in these TRANSACTIONS or in the Conference Records for the 1971 and 1972 Symposiums on the Theory and Applications of Multiple-Valued Logic Design. In particular, the result that follows for the case $n = 3$ is pertinent for applications in ternary switching theory.

II. AXIOMATIZATION

For completeness, the axioms given in [1] are repeated here.

Let n be a fixed integer ≥ 2 . Let L be a distributive lattice with zero 0 and unit 1, with the least upper bound of x and y denoted by $x \vee y$ and the greatest lower bound of x and y denoted by $x \wedge y$, and satisfying the following conditions.

Axiom 1: For every element $x \in L$ there exist n elements $C_0(x)$, $C_1(x)$, \dots , $C_{n-1}(x)$ which are pairwise disjoint and whose least upper bound is 1.

Axiom 2: There exist n fixed elements of L , denoted $0 = e_0$, $e_1, \dots, e_{n-2}, e_{n-1} = 1$ with the following properties.

Axiom 2a: The elements form a chain, with $e_{i-1} \leq e_i$ for $1 \leq i \leq n-1$.

Axiom 2b: If $x \in L$ and $x \wedge e_1 = 0$, then $x = 0$.

Axiom 2c: If $x \in L$ and, for some i , $x \vee e_{i-1} = e_i$, then $x = e_i$.

Axiom 3: For every $x \in L$,

$$x = [e_1 \wedge C_1(x)] \vee [e_2 \wedge C_2(x)] \vee \dots \vee$$

$$[e_{n-2} \wedge C_{n-2}(x)] \vee C_{n-1}(x).$$

To obtain the above in equational form, consider algebras $(L, \vee, \wedge, C_0, C_1, \dots, C_{n-1}, e_0, e_1, \dots, e_{n-1})$, where \vee and \wedge are binary operations, C_0, C_1, \dots, C_{n-1} are unary operations, and e_0, e_1, \dots, e_{n-1} are distinguished elements of the set L satisfying the following postulates for all x and y in L .

Postulate H1: The set L with the operations \vee and \wedge is a distributive lattice (see, for example, defining equations in [4, pp. 5, 35]).

Postulate H2: a) $e_0 \vee x = x$. b) $e_i \wedge e_j = e_i$ for $i \leq j$. c) $x \wedge e_{n-1} = x$.

Postulate H3: a) $C_i(x) \wedge C_j(x) = e_0$ for $i \neq j$. b) $C_0(x) \vee C_1(x) \vee \dots \vee C_{n-2}(x) \vee C_{n-1}(x) = e_{n-1}$.

Postulate H4: a) $C_i(x \vee y) = \{C_i(x) \wedge [C_0(y) \vee C_1(y) \vee \dots \vee C_i(y)]\} \vee \{C_i(y) \wedge [C_0(x) \vee C_1(x) \vee \dots \vee C_i(x)]\}$ for $i > 1$. b) $C_0(x \wedge y) = C_0(x) \vee C_0(y)$.

Postulate H5: $C_i(e_j) = e_0$ for $i \neq j$.

Postulate H6: $x = [e_1 \wedge C_1(x)] \vee [e_2 \wedge C_2(x)] \vee \dots \vee [e_{n-1} \wedge C_{n-1}(x)]$.

Theorem: Postulates H1 through H6 completely characterize Post algebras of order n .

Proof: If Postulates H1 through H6 hold, then Axioms 1, 2, and 3 follow. Note first that $C_i(e_i) = e_{n-1}$ follows directly from Postulate